The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A write-once memory device comprising a memory cell formed over an insulating surface, which includes a semiconductor film having at least two impurity regions and a region therebetween, an insulating film over the semiconductor film, a gate electrode formed over the region with [[an]] the insulating film interposed therebetween, and at least two wirings connected to the respective impurity regions,

wherein the semiconductor film interposed between the two wirings of the memory cell is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings,

~~wherein a potential of the gate electrode is changed,~~ and

~~wherein the gate electrode and the semiconductor film are formed in contact with the insulating film.~~

wherein the gate electrode has a gap over the region.

2. (Currently Amended) The write-once memory device according to claim 1, wherein [[each]] the memory cell of the write-once memory device comprises two or more gate electrodes on the same insulating film over the same semiconductor film.

3. (Canceled)

4. (Currently Amended) A write-once memory device comprising a first memory cell and a second memory cell formed over an insulating surface, each of which includes a semiconductor film having at least two impurity regions and a region therebetween, an insulating film on the semiconductor film, a gate electrode formed

over the region with [[an]] the insulating film interposed therebetween, and at least two wirings connected to the respective impurity regions,

wherein the first memory cell comprises an initial state[[; and]],

the semiconductor film interposed between the two wirings of the second memory cell is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings,

~~wherein a potential of the gate electrode is changed,~~ and

~~wherein the gate electrode and the semiconductor film are in contact with the insulating film.~~

wherein the gate electrode has a gap over the region.

5. (Currently Amended) The write-once memory device according to claim 4, wherein each of the first memory cell and the second memory cell of the write-once memory device comprises two or more gate electrodes on the same insulating film over the same semiconductor film.

6. (Canceled)

7. (Currently Amended) A write-once memory device comprising a memory cell formed over an insulating surface, which includes a semiconductor film having one or two impurity regions, an insulating film on the semiconductor film, [[an]] a gate electrode formed over the impurity region with [[an]] the insulating film interposed therebetween, and at least two wirings connected to the respective impurity regions or at least two wirings connected to the one impurity region,

wherein the semiconductor film interposed between the two wirings of the memory cell is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings,

~~wherein a potential of the gate electrode is changed,~~ and

~~wherein the gate electrode and the semiconductor film are in contact with the insulating film.~~

wherein the gate electrode has a gap over the impurity region.

8. (Previously Presented) The write-once memory device according to claim 7, wherein the gate electrode is interposed between the two wirings.

9. (Currently Amended) The write-once memory device according to claim 7, wherein [[each]] the memory cell of the write-once memory device comprises two or more gate electrodes on the same insulating film over the same semiconductor film.

10. (Canceled)

11. (Currently Amended) A write-once memory device comprising a first memory cell and a second memory cell formed over an insulating surface, each of which includes a semiconductor film having one or two impurity regions, an insulating film on the semiconductor film, [[an]] a gate electrode formed over the impurity region with [[an]] the insulating film interposed therebetween, and at least two wirings connected to the respective impurity regions or at least two wirings connected to the one impurity region,

wherein the first memory cell has an initial state[[; and]],

the semiconductor film interposed between the two wirings of the second memory cell is altered to an insulating state by applying a voltage between the gate electrode and at least one of the two wirings,

~~wherein a potential of the gate electrode is changed,~~ and

~~wherein the gate electrode and the semiconductor film are in contact with the insulating film.~~

wherein the gate electrode has a gap over the impurity region.

12. (Currently Amended) The write-once memory device according to claim 11, wherein the gate electrode is interposed between the two wirings.

13. (Currently Amended) The write-once memory device according to claim 11, wherein each of the first memory cell and the second memory cell of the write-once memory device comprises two or more electrodes on the same insulating film over the same semiconductor film.

14. (Canceled)

15. (Currently Amended) A manufacturing method of a write-once memory device, comprising the steps of:

forming an island shape semiconductor film over an insulating surface;

forming a gate insulating film over the island shape semiconductor film;

forming a gate electrode over the gate insulating film;

doping an N-type impurity element with the gate electrode used as a mask, thereby forming an N-type high concentration impurity region in the island shape semiconductor film;

forming an interlayer film over the gate insulating film and the gate electrode;

forming a contact hole in the interlayer film and a wiring connected to the N-type high concentration impurity region, thereby forming a memory cell[[,]]; and

applying a voltage between the gate electrode and the wiring of the memory cell, thereby altering a channel region of the island shape semiconductor film to an insulating state,

~~wherein a potential of the gate electrode is changed, and~~

~~wherein the gate electrode and the semiconductor film are in contact with the gate insulating film.~~

wherein the gate electrode has a gap over the island shape semiconductor film.

16. (Currently Amended) The manufacturing method of a write-once memory device according to claim 15, wherein [[each]] the memory cell of the write-once memory device comprises two or more gate electrodes on the same insulating film over the same island shape semiconductor film.

17. (Previously Presented) The write-once memory device according to claim 1, further comprising sidewalls formed on side surfaces of the gate electrode.

18. (Previously Presented) The write-once memory device according to claim 4, further comprising sidewalls formed on side surfaces of the gate electrode.

19. (Previously Presented) The write-once memory device according to claim 7, further comprising sidewalls formed on side surfaces of the gate electrode.

20. (Previously Presented) The write-once memory device according to claim 11, further comprising sidewalls formed on side surfaces of the gate electrode.

21. (Currently Amended) The manufacturing method of a write-once memory device according to claim 15, further comprising a step of forming sidewalls on side surfaces of the gate electrode.

22. (New) A write-once memory device comprising:

a first memory cell formed over an insulating surface, and comprising a first semiconductor film having at least two first impurity regions and a first region therebetween, a first insulating film over the first semiconductor film, a first gate

electrode formed over the first region, and at least two first wirings connected to the respective first impurity regions; and

a second memory cell formed over the insulating surface, and comprising a second semiconductor film having at least two second impurity regions and a second region therebetween, a second insulating film over the second semiconductor film, a second gate electrode formed over the second region, and at least two second wirings connected to the respective second impurity regions,

wherein the first region is altered to an insulating state and the second region is maintained in an initial state when applying a gate voltage to the first gate electrode and the second gate electrode, a first voltage to at least one of the two first wirings, and a second voltage to at least one of the two second wirings, and

wherein the first voltage is lower than the second voltage.